What is claimed is:

1. A method of forming a gate for a FinFET comprising the steps of:

forming a first mandrel over a substrate fin substantially perpendicular to the semiconductor fin, the mandrel having a first and second sidewalls perpendicular to the substrate;

forming a first sidewall spacer on the first sidewall;

removing the first mandrel;

depositing a second mandrel over the substrate, the semiconductor fin and the first sidewall spacer;

removing the first sidewall spacer thereby creating a first cavity extending through the second mandrel and exposing the semiconductor fin; and

forming a first gate conductor within the first cavity.

2. The method of claim 1, further comprising the steps of:

forming and a second sidewall spacer on the second sidewall;

depositing the second mandrel over the second sidewall spacer;

removing the second sidewall spacer thereby creating a second cavity extending through the second mandrel and exposing the semiconductor fin; and

forming a second gate conductor within the second cavity.

3. The method of claim 2, wherein the step of forming the first sidewall spacer and the second sidewall spacer further includes the steps of:

growing a first sidewall film on the first sidewall and a second sidewall film on the second sidewall;

selectively removing portions of the first sidewall film thereby leaving the first spacer straddling the semiconductor fin; and

selectively removing portions of the second sidewall film thereby leaving the second spacer straddling the semiconductor fin.

4. The method of claim 2, further comprising the step of:

forming respective gate dielectric material within the first and second cavities on the exposed semiconductor fin, before forming the respective gate conductor in each of the first and second cavities.

5. The method of claim 1, further comprising the step of:

removing the second mandrel.

6. The method of claim 2, wherein the step of depositing the second mandrel further includes the step of planarizing the second mandrel to a height that exposes the first and second sidewall spacers.

7. The method of claim 1, further comprising the step of:

forming a protective film on a top surface of the semiconductor fin.

8. The method according to claim 4, wherein the step of depositing respective gate dielectric material further includes the step of:

removing any protective film within the first and second cavities before forming gate dielectric material.

9. The method of claim 3, wherein the step of growing the first sidewall film and second sidewall film include the step of growing each respective film to a thickness equal to a desired channel length for the FinFET.

10. The method of claim 3, further comprising the step of:

removing any material that grows on a top surface of the first mandrel during performance of the steps of growing the first and second sidewall films.

11. A semiconductor device fabricated according to a process comprising the steps of:

forming a first mandrel over a substrate and a semiconductor fin substantially perpendicular to the semiconductor fin, the mandrel having a first and second sidewalls perpendicular to the substrate;

forming a first sidewall spacer on the first sidewall and a second sidewall spacer on the second sidewall;

removing the first mandrel;

depositing a second mandrel over the substrate, the semiconductor fin and the first and second sidewall spacers;

removing the first and second sidewall spacers thereby creating a first cavity and a second cavity extending through the second mandrel and exposing the semiconductor fin; and

forming a respective gate within each of the first and second cavities.

12. The semiconductor device of claim 11, wherein the process further comprises the steps of:

growing a first sidewall film on the first sidewall and a second sidewall film on the second sidewall;

selectively removing portions of the first sidewall film thereby leaving the first spacer straddling the semiconductor; and

selectively removing portions of the second sidewall film thereby leaving the second spacer straddling the semiconductor fin.

13. The method of claim 12, wherein the step of growing the first sidewall film and second sidewall film include the step of growing each respective film to a thickness equal to a desired channel length for the FinFET.

14. An intermediate structure formed during fabrication of a FinFET gate, the intermediate structure comprising:

a planarized mandrel layer covering a semiconductor fin formed on a substrate;

a first cavity extending vertically through the planarized mandrel layer thereby exposing a first portion of the semiconductor fin and substrate, said cavity having a width that determines a channel length of a first gate portion of the FinFET; and

a first gate conductor deposited within the first cavity.

15. The intermediate structure of claim 14, further comprising:

the semiconductor fin; and

a nitride cap formed over the semiconductor fin.

16. The intermediate structure of claim 14, further comprising:

a second cavity extending vertically through the planarized mandrel layer thereby exposing a second portion of the semiconductor fin and substrate, said cavity having a width that determines a channel length of a second gate portion of the FinFET; and

a second gate conductor deposited within the second cavity.

17. The intermediate structure of claim 14, further comprising a gate dielectric material separating the semiconductor fin and the first gate conductor.

18. The intermediate structure of claim 14, wherein:

the first cavity has a thickness substantially equal to an oxide sidewall spacer grown on an oxide mandrel overtop of the semiconductor film.

19. The intermediate structure of claim 18, wherein:

the thickness is less than a feature size attainable using optical projection lithography.